IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

C. Amendments to the Claims.

1. (Currently Amended) A memory cell, comprising:

a first node for storing a first potential;

a second node for storing a second potential; ~~**and**~~

transistor gates formed from a gate layer; and

a capacitor having plates coupled between the first node and second node, a portion of at least one plate of the capacitor comprising a first interconnect wiring **formed over the gate layer and includes a plurality of conductive layers** that interconnects circuit components of the memory cell.

2. (Original) The memory cell of claim 1, further comprising:

a first inverter having an input coupled to the first node and an output coupled to the second node; and

a second inverter having an input coupled to the second node and an output coupled to the first node; wherein

the first node stores a true data value and the second node stores a complementary data value.

3. (Original) The memory cell of claim 1, further including:

a first access transistor coupled to the first node; and

a second access transistor coupled to the second node.

4. (Cancelled) The memory cell of claim 1, further including:

transistor gates formed from a gate layer; and

the first conductive interconnect wiring is formed over the gate layer and includes a plurality of conductive layers, at least one of the conductive layers forming at least a portion of a first plate of the capacitor.

5. (Currently Amended) The memory cell of claim **41**, wherein:

the first conductive interconnect wiring includes a bottom conductive layer, a dielectric layer formed over the bottom conductive

layer, and a top conductive layer formed over the dielectric layer, the top conductive layer forming at least a portion of the first plate of the capacitor.

6. (Currently Amended) The memory cell of claim **41**, further including:

a second conductive interconnect wiring formed over the first conductive interconnect wiring that forms at least a portion of a second plate of the capacitor.

7. (Original) The memory cell of claim 6, wherein:

the second conductive interconnect wiring comprises titanium;

the bottom conductive layer comprises titanium nitride; and

the top conductive layer comprises titanium.

8. (Withdrawn) A method of forming a capacitor in an integrated circuit, comprising the steps of:

depositing an insulating layer over a plurality of capacitor structures, each capacitor structure comprising a dielectric layer disposed between a first interconnect layer and a second interconnect layer;

forming a recess in the insulating layer according to a capacitor mask pattern to expose the second interconnect layer of at least two capacitor structures; and

forming a third interconnect layer within the recess that is in electrical contact with the exposed second interconnect layers of the at least two capacitor structures.

9. (Currently Amended) The method of claim ~~7~~**8**, wherein:

the insulating layer comprises silicon oxide.

10. (Currently Amended) The method of claim ~~7~~**8**, wherein:

the third interconnect layer comprises titanium.

11. (Withdrawn) The method of claim 8, further including:

prior to depositing the insulating layer

forming the first interconnect layer;

forming the dielectric layer over the first interconnect layer;

forming the second interconnect layer over the dielectric layer; and

etching through the first interconnect layer, the dielectric layer, and the second interconnect layer to form the capacitor structures.

12. (Withdrawn) The method of claim 11, wherein:

the first interconnect layer comprises titanium nitride; and

the second interconnect layer comprises titanium.

13. (Withdrawn) The method of claim 11, wherein:

after forming the capacitor structures

depositing a spacer insulating layer over the capacitor structures; and

anisotropically etching the spacer insulating layer to form insulating spacers on side surfaces of the capacitor structures while exposing the second interconnect layer of the capacitor structures.

14. (Withdrawn) The method of claim 8, further including:

the step of forming a recess in the insulating layer includes etching a portion of the first insulating layer; and

after forming the third interconnect layer, chemical-mechanical polishing to remove portions of the third interconnect layer outside of the recess.

15. (Withdrawn) A method of forming an integrated circuit memory cell, comprising the steps of:

forming a first interconnect wiring that electrically connects a plurality of transistor gates to transistor diffusion regions, the first interconnect wiring pattern comprising at least one dielectric layer between top and bottom conductive layers; and

forming a second interconnect layer over the first interconnect wiring in electrical contact with the top conductive layers to form a capacitor, the capacitor including a first plate comprising the top conductive layer, a second plate comprising the second interconnect layer, and a capacitor dielectric comprising the at least one dielectric layer.

16. (Withdrawn) The method of claim 15, wherein:

the step of forming the first interconnect wiring includes

forming the bottom conductive layer having a thickness of no more than about 1000 angstroms;

forming the at least one dielectric layer having a total thickness of less than about 80 angstroms;

forming the top conductive layer having a thickness of no more than about 300 angstroms; and

etching through the bottom conductive layer, at least one dielectric layer and the top conductive layer according to a first wiring pattern.

17. (Withdrawn) The method of claim 15, further including:

forming insulating sidewalls on the sides of the first interconnect wiring.

18. (Withdrawn) The method of claim 17, wherein:

the step of forming insulating sidewalls includes

depositing a layer of silicon nitride having a thickness of no more than about 500 angstroms; and

anisotropically etching the layer of silicon nitride.

19. (Withdrawn) The method of claim 15, wherein:

the first interconnect wiring includes

a first wiring portion that electrically connects a gate of at least a first memory cell transistor to a source/drain region of a second memory cell transistor, and

a second wiring portion that electrically connects a gate of at least a second memory cell transistor to a source/drain region of the first memory cell transistor.

20. (Withdrawn) The method of claim 19, wherein:

the first and second wiring portions are formed on an interconnect insulator layer;

the first wiring portion is electrically connected to the gate of the first memory cell transistor by a first local contact that extends through the interconnect insulator layer; and

the second wiring portion is electrically connected to the gate of the second memory cell transistor by a second local contact that extends through the interconnect insulator layer.